Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended and new claims added to clarify Applicants disclosed and claimed invention.

Support for the amended claims is found in the original claims and/or the Specification. No new matter has been added.

For example, support for new claims 22-30 is found in the Specification in the original claims as well as Figures 5, 6, 11 and 12, and at paragraph 0033:

"Fig. 6 shows a patterned second conductor layer 28a/b nested within a patterned second barrier layer 26a/b in turn planarized within the blanket capacitor dielectric layer 24. Shown in phantom outline beneath the blanket capacitor dielectric layer 24 is the patterned first conductor layer 18a nested within the patterned first barrier layer 16a. Also shown in phantom is the patterned first conductor layer 18b/c/d nested within the patterned first barrier layer 16b/c/d. As is illustrated within Fig. 5 and Fig. 6, the patterned first conductor layer 18b/c/d is formed in the **shape of a comb with the series of tines** 18b, 18c and 18d horizontally separated by the pair of second apertures 23a and 23b. The patterned second conductor layer 28a/b fills the pair of

second apertures 23a and 23b and provides a pair of second tines horizontally (and not vertically) interdigitated with the series of first tines."

Claim Rejections under 35 USC 103(a)

1. Claims 1-2 and 6 stand rejected under 35 USC 103(a) as unpatentable over Johnson et al. (US 6,441,419).

Johnson et al. disclose a **vertically interdigitated capacitor** between an upper interconnect layer and a lower interconnect layer (see Abstract; Figure 1). The capacitor dielectric material (item 44) is disposed between vertically interdigitated capacitor plates also functioning as barrier layers (items 42 and items 46; e.g., col 5, lines 35-54). The upper and bottom capacitor plates are disclosed to be formed of a barrier layer material (col 5, lines 65-67; col 6, lines 53-62) to completely encapsulate upper metal fill portions (item 60) **and lower metal fill portions** (item 38) forming separate lower conductor portions (item 38).

In a second embodiment, Johnson et al. disclose a capacitor structure which has a contiguous upper plate portion/barrier layer (item 56a; Figure 13), **separate lower U-shape plate portions** (item 52) and **separate U-shaped capacitor dielectric portions** (item 44) between the lower U-shaped plates and the upper contiguous plate portion (56a) (see e.g., col 13, lines 28-41). A lower level conductor (38b) portion contiguous horizontally. In this embodiment "the capacitor 32 does not include any portions of the upper plate" (item 56 Fig 13 "adjacent to the vertical legs of the lower U-shaped portions (item 52) in the spaces between the horizontally spaced lower U-shaped portions 52" (see col 13, lines 49-52).

Thus, Johnson et al. disclose a different structure than Applicants disclosed and claimed invention. Johnson et al. do not disclose several aspects of Applicants disclosed and claimed invention including:

"a first capacitor plate layer disposed over the substrate, the first capacitor plate layer comprising a horizontally separated and contiguously interconnected first series of tines;

a second capacitor plate layer separated from the first capacitor plate layer by a capacitor dielectric layer, the second capacitor plate layer comprising a horizontally separated and interconnected second series of tines horizontally interdigitated between the horizontally separated and interconnected first series of tines, wherein the capacitor dielectric layer is a single contiguous serpentine shaped dielectric layer wherein said first series of tines and said second series of tines are horizontally but not vertically interdigitated to form opposing sidewall portions; "

In a first embodiment (see Figure 1) Johnson et al. Johnson et al. teach away from Applicants invention by teaching and disclosing a **vertically interdigitated** capacitor (see abstract) where the first and second series of tines are vertically interdigitated. (see Figure 1). In the second embodiment of

Johnson et al. (see Figure 13), disclose a capacitor that appears horizontally interdigitated but is formed the by **separated U-shaped lower plate portions and separated U-shaped capacitor plate portions.**

In contrast with Applicants disclosed and claimed invention, Johnson et al. does not disclose several aspects of Applicants disclosed and claimed invention including:

"a first capacitor plate layer disposed over the substrate, the first capacitor plate layer **comprising a horizontally separated and contiguously interconnected first series of tines disposed on a dielectric layer;**

Johnson et al. also does not disclose:

a second capacitor plate layer separated from the first capacitor plate layer by a **contiguous serpentine shaped capacitor dielectric layer,** the second capacitor plate layer comprising a horizontally separated and contiguously

interconnected second series of tines, said second series of tines horizontally interdigitated between the first series of tines."

On the other hand, Jones et al. disclose an interdigitated capacitor where a contiguous **bottom conductive layer** is disposed in contact with **separately formed first electrodes** on the conductive layer to form a comb shaped structure (see col 2, lines 26-36). A capacitor dielectric (item 510, Fig 5) is then formed to cover the electrodes (item 310) and exposed portions of the **bottom conductive layer** item 120) (see col 4, lines 52-61). Second electrodes (item 610, Figure 6) are them formed to cover the capacitor dielectric and fill interdigitated spaces between the first electrodes (col 5, lines 10- 19) followed by **forming a separate upper conductive layer** (item 620) to contact exposed portions of the second electrodes.

In another embodiment the upper and lower conductive layers are not formed so that the capacitor dielectric **is formed only between separately formed first and second electrodes to make**

multiple capacitors (see col 2, lines 16-25; col 5, lines 38-48).

There is no apparent motivation for combining the teachings of Johnson et al. who teach either a **vertically interdigitated damascene structure** with **separate u-shaped conductive portions (item 38 Fig 1) underlying a contiguous lower** plate/barrier layer (items 42, 52 Figure 1) **or** a horizontally interdigitated damascene structure with **separate U-shaped lower plate** (electrode portions) (item 52; Figure 13) with the teachings of Jones et al. who teach a completely different non-damascene capacitor structure where the upper and lower conductor layers (items 120 and 620 Fig 6) connect to noncontiguous **horizontally interdigitated** upper and lower electrodes extending from the respective underlying and overlying conductor layers.

For example in the horizontally interdigitated structure (Figure 13), Johnson et al. teach directly away from the structure of Jones et al. by teaching "the capacitor 32 does not include any portions of the upper plate" (item 56 Fig 13

"adjacent to the vertical legs of the lower U-shaped portions (item 52) in the s-aces between the horizontally spaced lower U-shaped portions 52" (see col 13, lines 49-52).

In addition, any modification of Johnson et al. or Jones et al. to achieve Applicants disclosed and claimed invention would change the principal of operation of the structures of either and make both Johnson et al. and Jones et al. unsuitable for their intended operation.

Even assuming *arguendo* proper motivation for combination of the teachings of Johnson et al. and Jones et al., such combination does not produce Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re*

Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended

purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

Neither Johnson et al. nor Jones et al., either individually or in combination, make out a *prima facie* case of obviousness with respect to Applicants independent claims therefore likewise failing with respect to dependent claims.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

U.S.S.N. 10/804,899

Respectfully submitted,

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